Patent Claims

1. Nonvolatile semiconductor storage element with a semiconductor substrate (1) in which a source region (S), a drain region (D) and an intermediate channel region are formed;
a control layer (5) which is formed on a first part section (I) of the channel region and is insulated from this by a first insulating layer (2A);
a charge storage layer (3A, 3B) which is formed on a second part section (IIA, IIB) of the channel region and is insulated from that by a second insulating layer (2BA, 2BB); and
a programming layer (6A, 6B) which is formed on the charge storage layer (3A, 3B) and is insulated from that by a third insulating layer (4A, 4B), characterized by an interconnect layer (6AA, 6BB) for electrically connecting the programming layer (6A, 6B) to the source region (S) or drain region (D).

2. Nonvolatile semiconductor storage element according to Claim 1, characterized in that the second part section of the channel region has a source side part section (IIB) and a drain side part section (IIA);
the charge storage layer has a source side charge storage layer (3B) and a drain side charge storage layer (3A);
the programming layer has a source side programming layer (6B) and a drain side programming layer (6A); and
the interconnect layer has a source side interconnect layer (6BB) and a drain side interconnect layer (6AA), the source side interconnect layer (6BB) electrically connecting the source side programming layer (6B) to the source region (S) and the drain side interconnect layer (6AA) electrically connecting the drain side programming layer (6A) to the drain region (D).

3. Nonvolatile semiconductor storage element according to Claim 1 or 2, characterized in that the

charge storage layer (3A, 3B) represents an electrically nonconductive layer.

4. Nonvolatile semiconductor storage element according to one of Claims 1 to 3, characterized in that the first and second insulating layer (2A, 2BA, 2BB) exhibits SiO_2.

5. Nonvolatile semiconductor storage element according to one of Claims 1 to 4, characterized in that the charge storage layer (3A, 3B) exhibits an Si_3N_4, HFO_2 or ZrO_2 layer.

6. Nonvolatile semiconductor storage element according to one of Claims 1 to 5, characterized in that the control layer (5), the programming layer (6A, 6B) and the interconnect layer (6AA, 6BB) have doped polysilicon.

7. Method for producing a nonvolatile semiconductor storage element with the following steps:

a) preparing a semiconductor substrate (1);

b) forming a first insulating layer (2A) on the surface of the semiconductor substrate (1);

c) forming and patterning a control layer (5) on the surface of the first insulating layer (2A);

d) forming a sequence of layers consisting of a second insulating layer (2B), a charge storage layer (3) and a third insulating layer (4) on the surface of the semiconductor substrate (1) and of the patterned control layer (5);

e) forming and patterning a programming layer (6A, 6B) on the third insulating layer (4) on the side walls of the patterned control layer (5);

f) forming source regions (S) and drain regions (D) in the semiconductor substrate (1) by using the patterned programming layer (6A, 6B) and the patterned control layer (5) as a mask;

g) patterning the third insulating layer (4), the charge storage layer (3) and the second insulating layer (2B) by using the patterned programming layer (6A, 6B) as a mask;

h) forming a fourth insulating layer (7) on the surface of the semiconductor substrate (1), of the patterned programming layer (6A, 6B) and of the patterned control layer (5);

i) exposing interconnect areas at least of parts of the patterned programming layer (6A, 6B), of the source region (S) and of the drain region (D); and

j) forming an electrically conductive interconnect layer (6AA, 6BB) in the exposed interconnect areas for contacting the programming layer (6A, 6B) of the source region (S) and of the drain region (D).

8. Method according to Claim 7, characterized in that a gate dielectric is formed as the first insulating layer (2A) in step b).

9. Method according to Claim 7 or 8, characterized in that a first polysilicon layer is deposited as control layer (5) in step c).

10. Method according to one of Claims 7 to 9, characterized in that an ONO sequence of layers is deposited in step d).

11. Method according to one of Claims 7 to 10, characterized in that a spacer method is performed for depositing and patterning a second polysilicon layer as programming layer (6A, 6B) in step e).

12. Method according to one of Claims 7 to 11, characterized in that an ion implantation and a thermal post-treatment is performed for diffusing-out and activating the source and drain regions (S, D) in step f).

13. Method according to one of Claims 7 to 12, characterized in that an anisotropic dry etching of the sequence of layers and an isotropic etching-back of at least the charge storage layer (3) is performed for forming charge storage layer recesses in step g).

14. Method according to Claim 13, characterized in that an oxide deposition is performed for filling up the charge storage layer recesses in step h).

15. Method according to one of Claims 7 to 14, characterized in that a third polysilicon layer is deposited and planarized as interconnect layer (6AA, 6BB) in step j).

16. Method for writing an information item into a nonvolatile semiconductor storage element according to one of Claims 2 to 6, with the following steps:

a) applying a first positive write voltage to the source side interconnect layer (6BB);

b) applying a second positive write voltage, which is much higher than the first positive write voltage, to the drain side interconnect layer (6AA); and

c) applying a third positive write voltage, which is slightly higher than the RMS threshold voltage of a respective inner transistor, to the control layer (5) for generating an SSI condition.

17. Method for erasing an information item in a nonvolatile semiconductor storage element according to one of Claims 2 to 6, comprising the following steps:

a) applying a floating potential to the source side interconnect layer (6BB);

b) applying a high first erase voltage to the drain side interconnect layer (6AA); and

c) applying a second erase voltage, which is lower than the RMS threshold voltage of a respective inner transistor, to the control layer (5) for generating an avalanche effect condition.

18. Method for reading an information item in a nonvolatile semiconductor storage element according to one of Claims 2 to 6, comprising the following steps:

a) applying a first positive read voltage to the source side interconnect layer (6BB);

b) applying a second read voltage, which is sufficiently smaller than the first read voltage, to the drain side interconnect layer (6AA); and

c) applying a third read voltage, which is in the region of the first read voltage, to the control layer (5) for generating a reverse readout.